WHAT IS CLAIMED:

1. A circuit for monitoring the state of at least one switch, comprising:

a first circuit, coupled to a switch, for detecting whether the switch is in one of a closed state and an open state and generating a signal having a value based upon the detection; and

a second circuit, coupled to the first circuit, for configuring the first circuit to selectively detect the switch switching from a normally open state and to selectively detect the switch switching from a normally closed state.

2. The circuit of claim 1, wherein the first circuit includes a third circuit for detecting whether the switch changes from a closed state to an open state and for pulling a first terminal of the switch to a voltage representative of one of a logic high state and a logic low state.

3. The circuit of claim 2, wherein the third circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state.

4. The circuit of claim 3, wherein the third circuit comprises:

at least one resistive element;

a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source;

a second transistor coupled between the first terminal of the at least one resistive element and the first terminal of the switch;

a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and

a fourth transistor coupled between the second terminal of the at least one resistive element and the first terminal of the switch.

5. The circuit of claim 4, wherein the second circuit comprises control circuitry for activating the first transistor and the third transistor at substantially the same time, and activating the second transistor and the fourth transistor at substantially the same time.

6. The circuit of claim 5, wherein the control circuitry comprises a register.

7. The circuit of claim 5, wherein the second circuit comprises control circuitry for selectively activating one of the first transistor and the third transistor while occasionally activating the other of the first and third transistors, and for selectively activating one of the second transistor and the fourth transistor while occasionally activating the other of the second and fourth transistors.

8. The circuit of claim 1, wherein the first circuit includes a third circuit for detecting whether the switch changes from an open state to a closed state and for relatively

weakly pulling a first terminal of the switch towards a voltage representative of one of a logic high state and a logic low state.

9. The circuit of claim 8, wherein the third circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state.

10. The circuit of claim 9, wherein the third circuit comprises at least one first transistor coupled between a high reference voltage level and the first terminal of the switch, at least one second transistor coupled between a low reference voltage level and the first terminal of the switch, and control logic for generating at least one control signal having a value indicative of a configuration of the third circuit, a control terminal of each of the at least one first transistor and the at least one second transistor having a value based upon the value of the at least one control signal.

11. The circuit of claim 10, wherein the third circuit comprises a first detection circuit having an input coupled to the first terminal of the switch and an output coupled to a control terminal of the at least one first transistor, the at least one control signal being coupled to an input of the first detection circuit, the output of the first detection circuit having a value indicative of the first detection circuit detecting the first terminal of the switch being pulled to a voltage representative of a logic low level.

12. The circuit of claim 11, wherein the first detection circuit comprises a logic gate with hysteresis.

13. The circuit of claim 11, wherein the third circuit further comprises a second detection circuit having an input coupled to the first terminal of the switch and an output coupled to a control terminal of the at least one second transistor, the at least one control signal being coupled to an input of the second detection circuit, the output of the second detection circuit having a value indicative of the second detection circuit detecting the first terminal of the switch being pulled to a voltage representative of a logic high value.

14. The circuit of claim 13, wherein the third circuit further comprises an output circuit having a first input coupled to the output of the first detection circuit, a second input coupled to the output of the second detection circuit, and an output having a value representative of one of the first and second detection circuits detecting the switch being closed.

15. The circuit of claim 1, wherein the circuit further comprises:

a third circuit for detecting whether a second switch is in one of a closed state and an open state and generating a signal having a value based upon the detection; and

a fourth circuit, coupled to the third circuit, for configuring the third circuit to selectively detect the second switch switching from a normally open state and from a normally closed state.

16. A method for detecting the state of at least one switch using a circuit, comprising:

configuring the circuit to select whether the circuit is to detect a switch switching from a normally open state or from a normally closed state;

detecting, by the circuit, the switch switching from the selected state; and

generating a signal indicative of the detection.

17. The method of claim 16, wherein the step of configuring comprises configuring the circuit to select the circuit detecting the switch switching from the normally closed state, and to select, during the time the switch is normally closed, the circuit to relatively weakly pull a terminal of the switch towards a voltage representative of one of a logic high state and a logic low state.

18. The method of claim 17, wherein the step of configuring comprises activating transistors to couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state.

19. The method of claim 17, wherein the step of configuring comprises occasionally activating at least one transistor to occasionally couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state.

20. The method of claim 16, wherein the step of configuring comprises configuring the circuit to select the circuit detecting the switch switching from the normally open state, and to select, during the time the switch is normally open, the circuit to relatively weakly pull a terminal of the switch to a voltage representative of one of a logic high state and a logic low state.

21. A system, comprising:

a switch having a first conduction terminal and a second conduction terminal;

a first circuit coupled to the first conduction terminal of the switch, the first circuit being configurable to selectively detect the switch being in a closed state and to selectively detect the switch being in an open state.

22. The system of claim 21, wherein the first circuit is configurable to selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic high state, and to selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic low state.

23. The system of claim 22, wherein the first circuit selectively weakly pulls the first terminal of the switch towards a preselected logic state, relative to a drive strength of the switch to pull the first terminal thereof towards a different logic state.

24. The system of claim 23, wherein the first circuit comprises:

at least one resistive element;

a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source;

a second transistor coupled between the first terminal of the at least one resistive element and the first conduction terminal of the switch;

a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and

a fourth transistor coupled between the first conduction terminal of the switch and the second terminal of the at least one resistive element.

25. The system of claim 24, wherein the first circuit further comprises control circuitry for selectively activating the first and third transistors at substantially the same time, and selectively activating the second and fourth transistors at substantially the same time.

26. The system of claim 24, wherein the first circuit further comprises control circuitry for selectively activating one of the first and third transistors while occasionally activating the other of the first and third transistors, and for selectively activating one of the second and fourth transistors while occasionally activating the other of the second and fourth transistors.